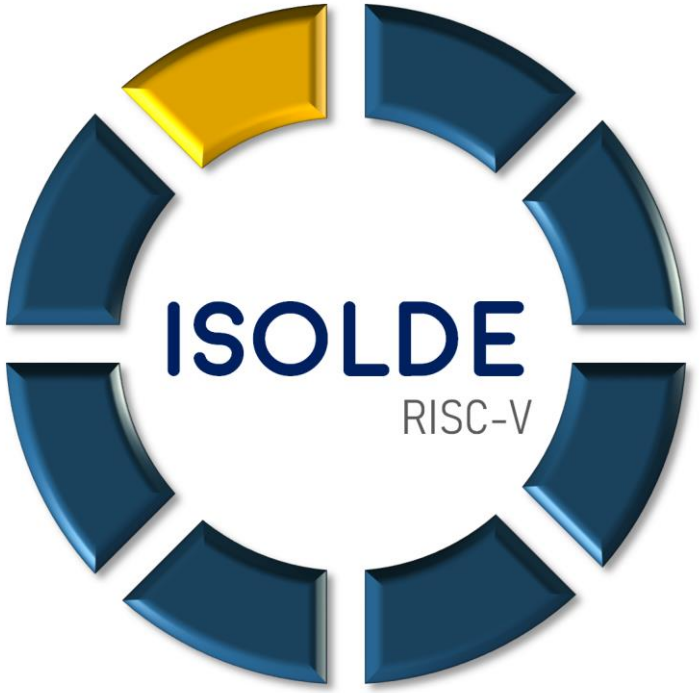


ISOLDE

HIgh Performance, Safe, Secure, Open-Source
Leveraged RISC-V Domain-Specific Ecosystems

Dataweek 2023 – Data meets Infrastructure at the Edge

Holger Schmidt, Infineon Technologies AG

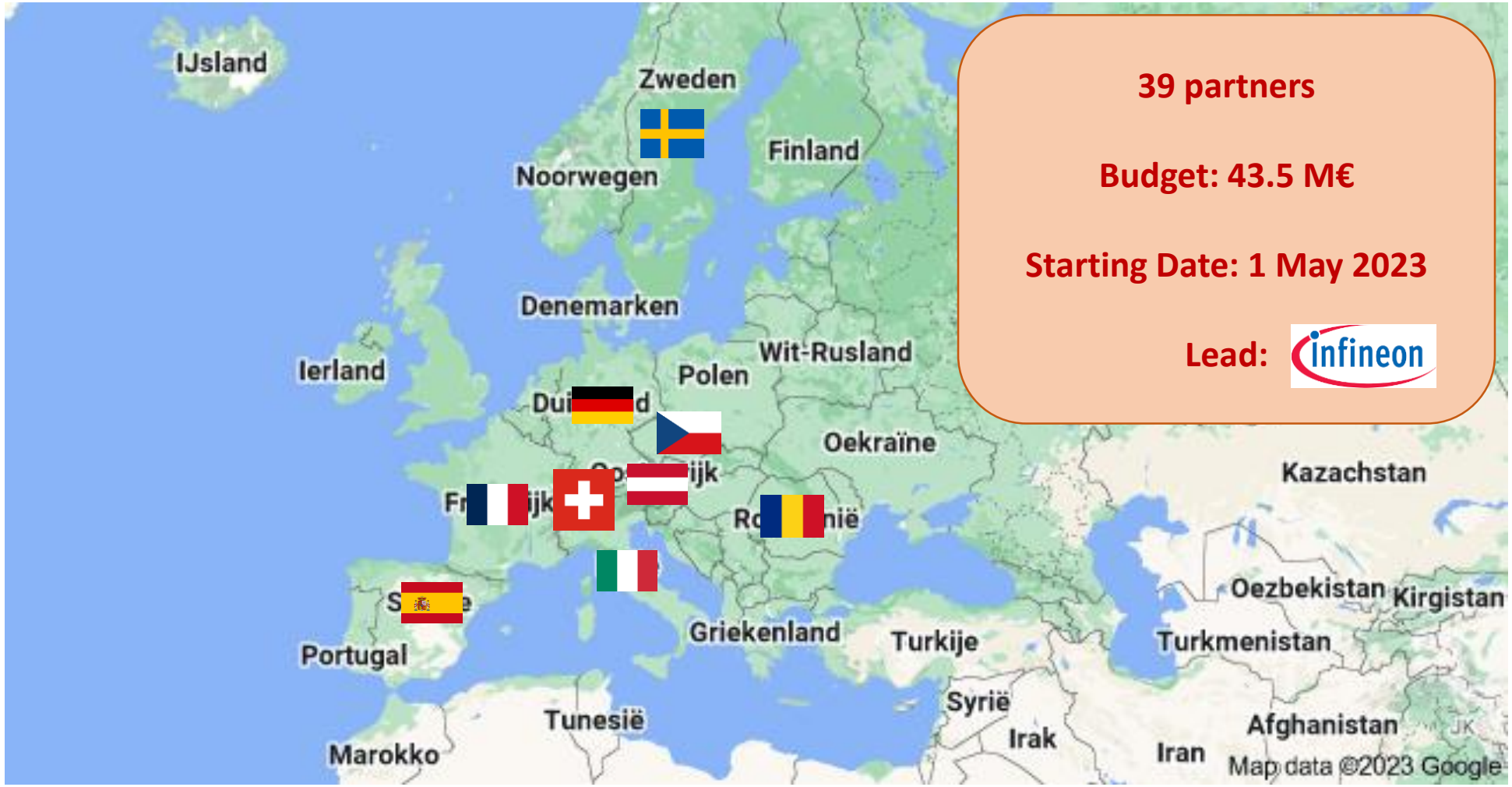
June 13 2023

European Commission

KDT JU
Key Digital Technologies Joint Undertaking

ISOLDE receives funding from the Key Digital Technologies Joint Undertaking under grant agreement nr. 101112274. The KDT JU receives support from the European Union's Horizon Europe research and innovation programme and its members Austria, Czechia, France, Germany, Italy, Romania, Spain, Sweden, Switzerland.

ISOLDE Consortium



39 partners

Budget: 43.5 M€

Starting Date: 1 May 2023

Lead: Infineon

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ISOLDE Aim and Approach

Ambition

- within five years, high-performance RISC-V CPUs achieve a comparable or better functional, performance, safety and security as well as power efficiency level than established competing architectures

Overall aim

- expand, mature, industrialize and make available the European high-performance RISC-V ecosystem so that it is able to compete with existing commercial/ proprietary alternatives

How

- exploring and implementing advanced architectures
- providing novel accelerators as well as IPs
- completing the high-performance compute infrastructure
- following and contributing to specifications from suitable industrial bodies and to Europe's long-term strategy for RISC-V based ecosystem
- creating an open-source repository of industrial quality components

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ISOLDE Objectives & Expected Impact

Specific Objectives	Expected Impacts after the project
Processor Development	At least 4 industrial SoC design starts per year, embedding high-end RISC-V multi-cores for a total amount of 12 targeted products in the 3 next years following the project end.
Industrial Quality SoC Components for HP Parallel Computing	At least 2 ISOLDE-originated components used in 4 industrial SoC design-ins over each of the first 3 years after the end of ISOLDE, for a total of at least 24 component design-ins. IP repository available and filled.
SoC Development Infra-Structure	Availability of HPC optimized SW stacks, SW development environment and EDA tools to design and verify RISC-V based SoC will cut the NRE cost for designing RISC-V based systems by 5%. The ISOLDE EDA flow will be used in 3 other European projects in the first 2 years after the end of ISOLDE.

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ISOLDE Objectives & Expected Impact

Specific Objectives	Expected Impacts after the project
Features enabling Safety and/or Security Certification for HP RISC-V Computing	Within 5 years after ISOLDE end, at least 50% of the ISOLDE HW and SW IPs will pass safety and security certification as required by their application domain.
Active European Embedded HP Computing Research	At least 5 new high-performance RISC-V architecture variants starting with ISOLDE technology will be available 4 years after the end of the project – potentially as results of projects contributing to subsequent calls; each being 10x faster than the ISOLDE cores at the end of the project.
Demonstration of Component Interoperability	At least 5 SoCs using ISOLDE's interoperable components will be available 4 years after project end.
High Quality Open-Source HW and SW	The open-source HW and SW content definition is accepted as de-facto standard 2 years after the end of ISOLDE and requested as mandatory in all subsequent calls.

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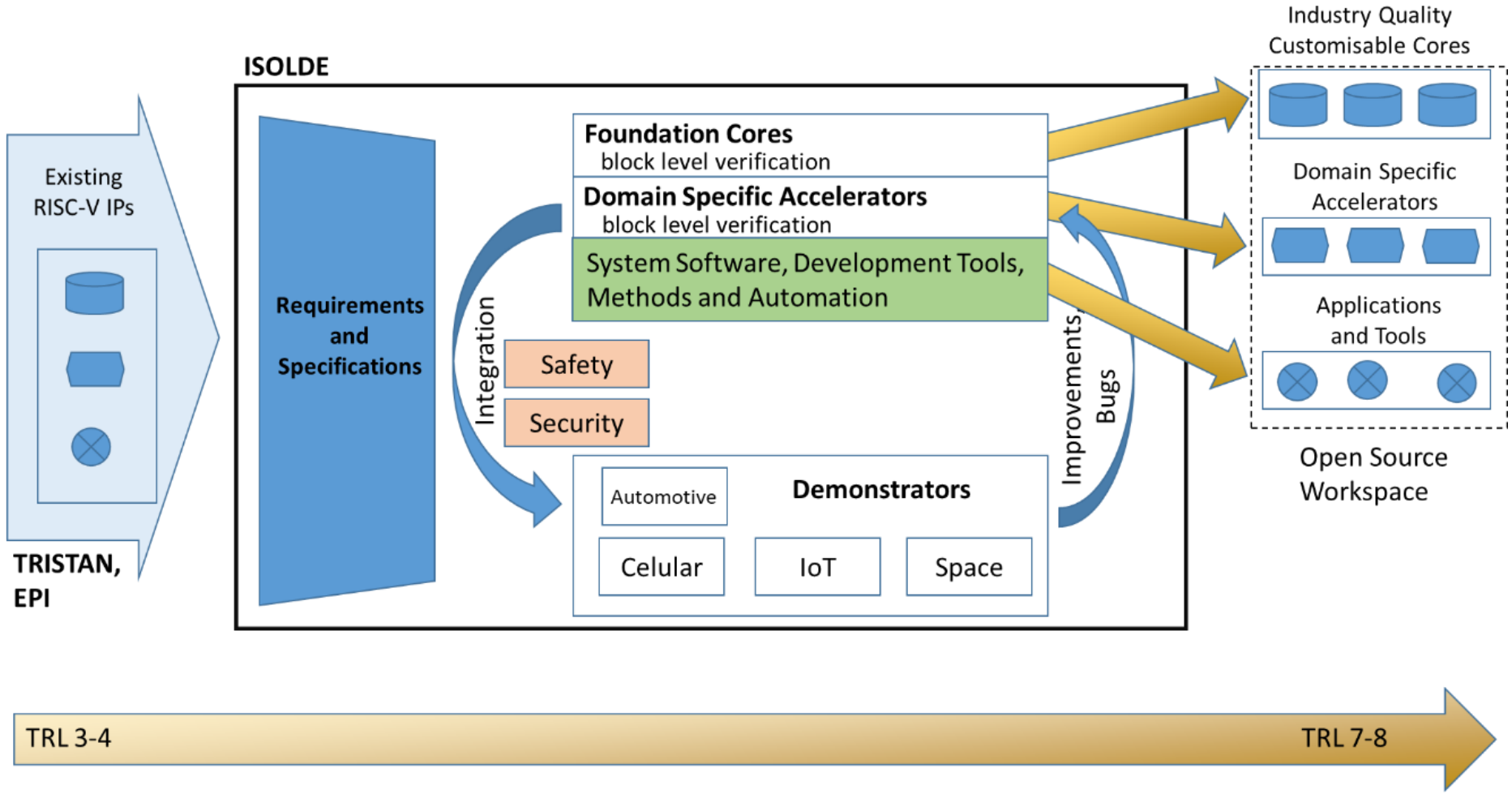
ISOLDE Scientific Methodology



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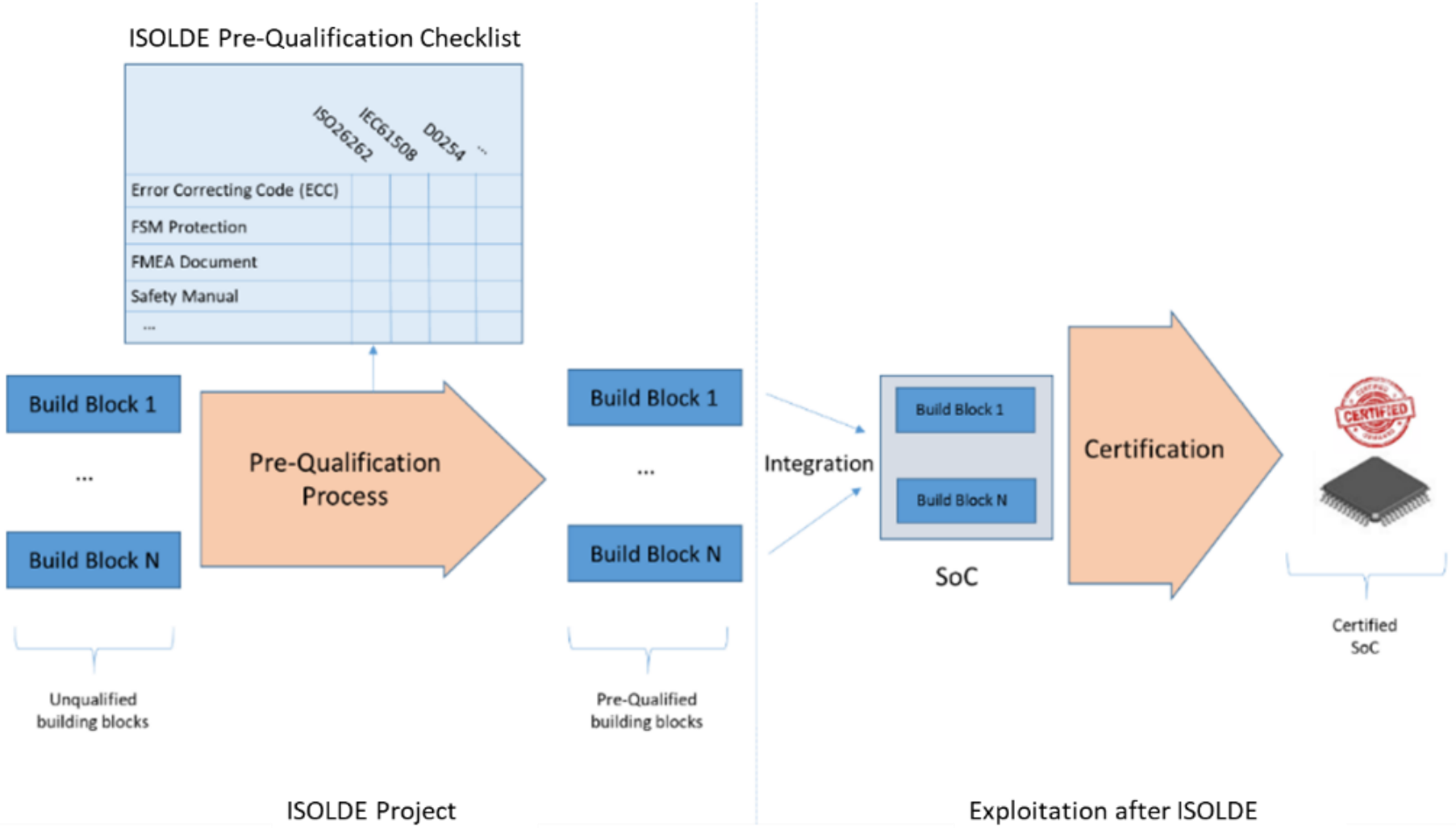
ISOLDE Pre-Certification Process



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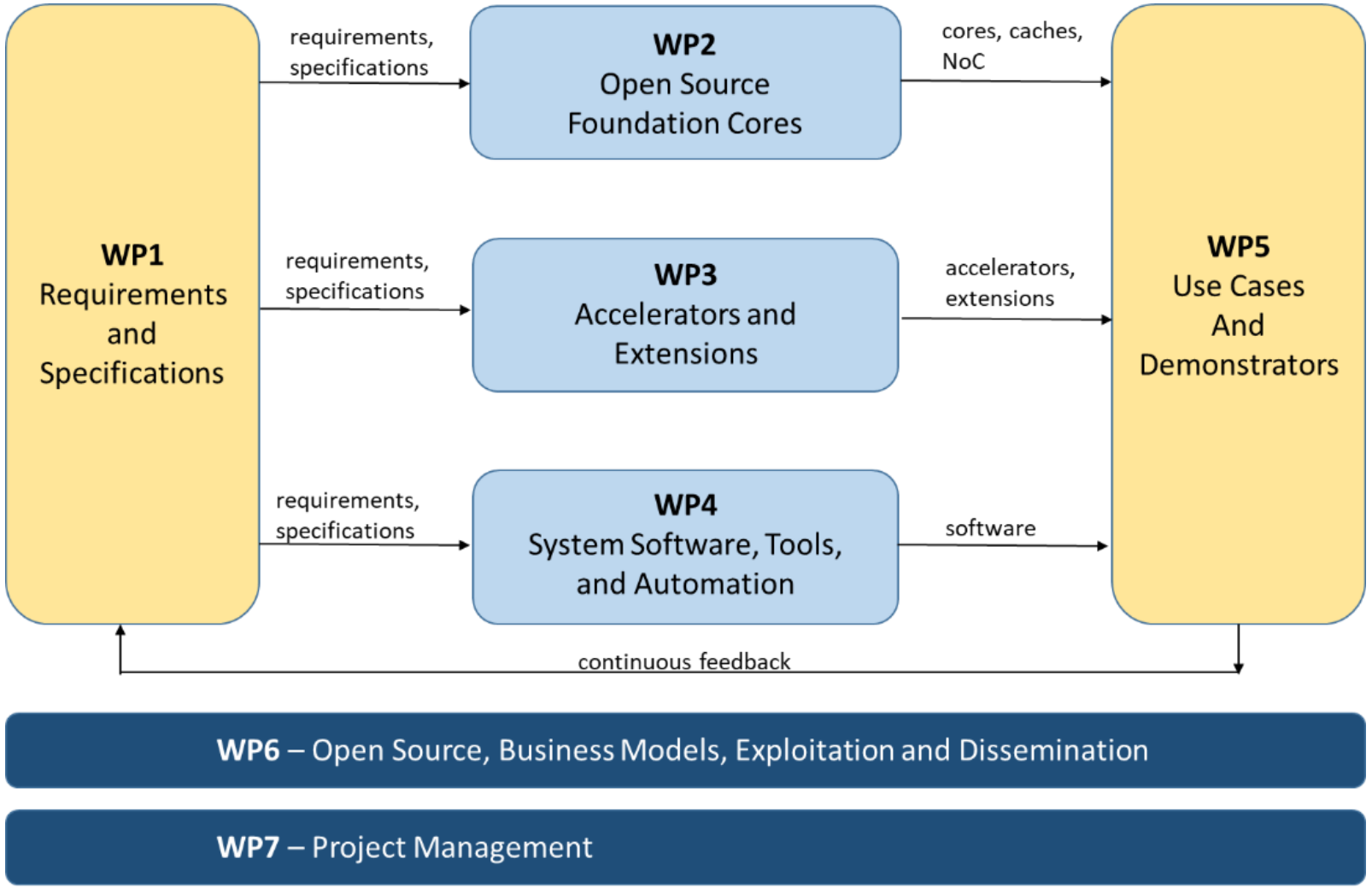
ISOLDE Project Structure



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ISOLDE Expected Results Hardware (Excerpt)

Foundation Cores

- CVA-6 & NOEL-V enhanced by cybersecurity extensions, templating tools, IF‘es to ISOLDE accelerators
- Interconnect components, e.g., fully piplined wormhole NoC
- ...

Accelerators and Extensions

- Mixed Precision FPU for ML, Vector unit with SIMD and multi-precision unit
- Safety Controller, Safety Island Interface
- AI accelerator and FP Tensor Processing Unit
- Scratchpad memories w/ deterministic access times for RT applications
- Root-of-Trust Unit, PCQ unit HW blocks
- ...

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ISOLDE Expected Results Software (Excerpt) & Demonstrators

System Software, Tools and Automation

- Low-level SW interfaces and their integration into Linux, PikeOS, XtratuM
- Fault injection toolkit
- Mixed precision compiler
- Analysis tools for embedded SW
- Power monitor generator toolset, power/performance prediction framework
- Malicious control-flow pattern detection utilizing a root-of-trust unit
- ...

Application Domains & Demonstrators

- Smart Home, Automotive, Space, IoT
- FPGA, FPGA & ready to TO SoC Design, FPGA & Testchip

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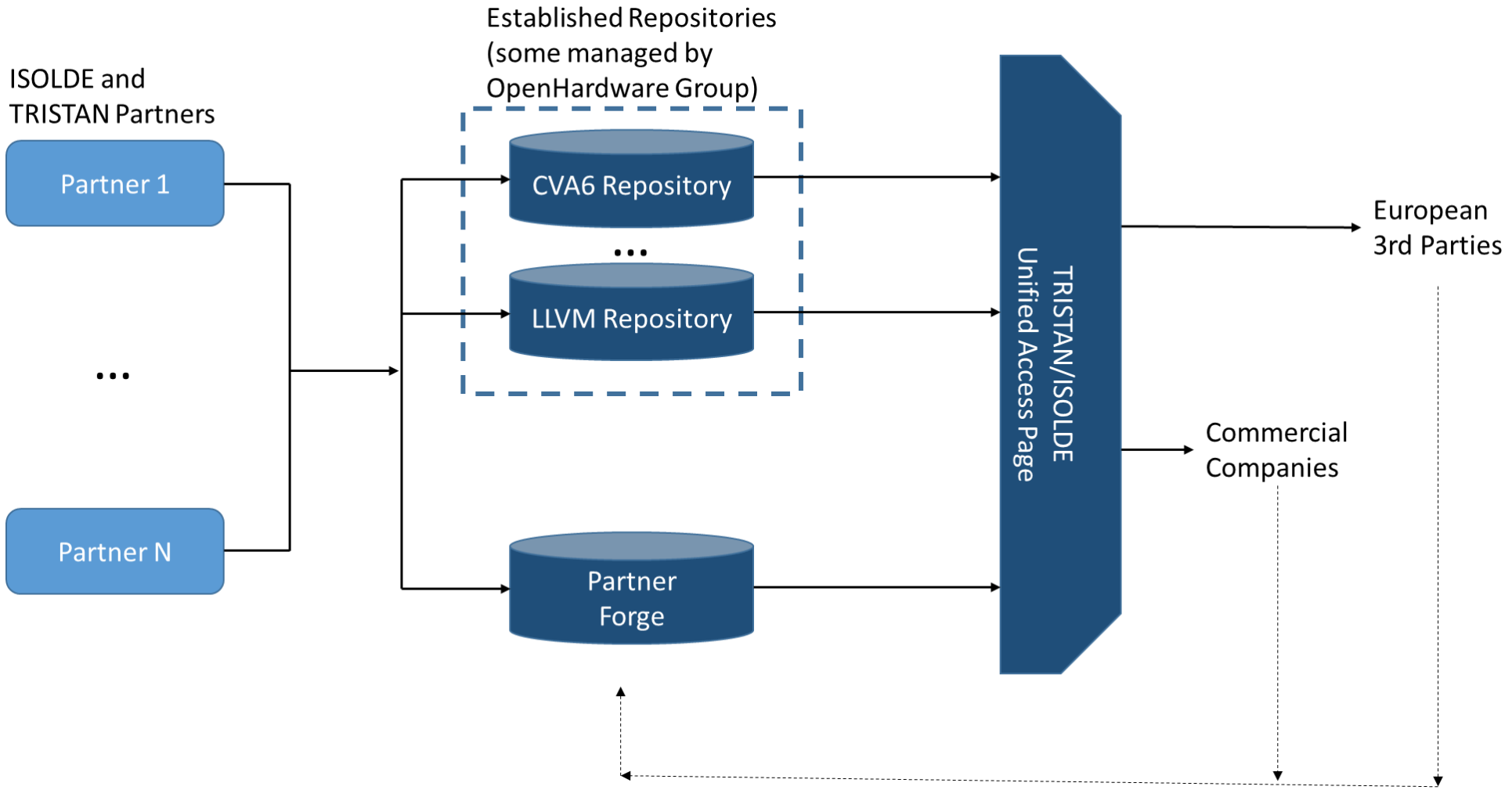
ISOLDE Virtual Repository



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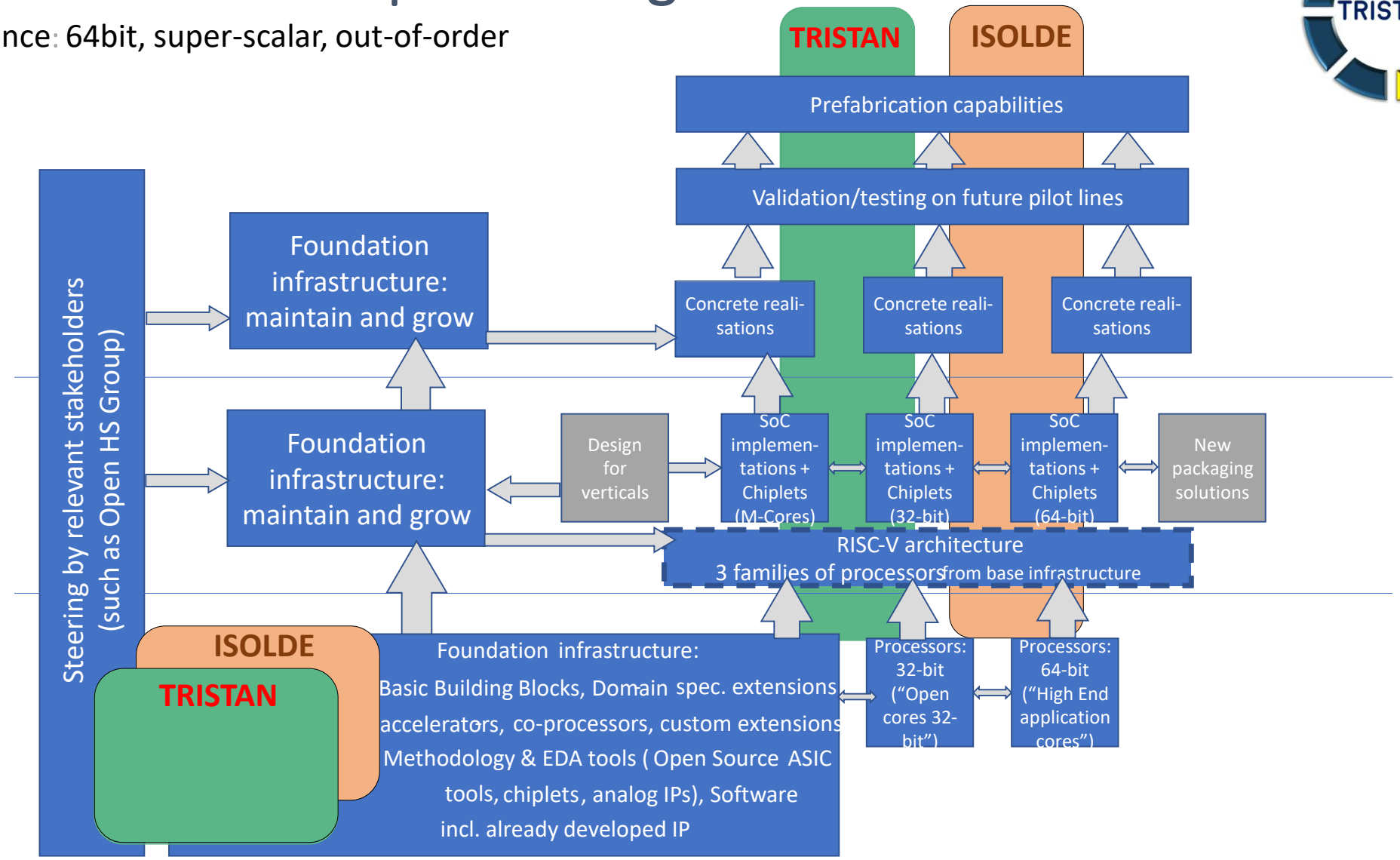
EU Vision - ISOLDE complementing TRISTAN

High Performance: 64bit, super-scalar, out-of-order



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TRISTAN and ISOLDE Project

Synergise, Complement and Build a strong European Network

Item	Tristan	Isolde	Comment
Processor Development	• Decent Performance • CVA6 and Pulp	• High Performance • CVA6, Noel-V	• To be proven in real designs • Isolde strives for super scalar, out of order, 64 bit
Building Blocks for SoC/High Perf, Computing	• SoC Buidling Blocks	• High performance and/or low power accelerators	• In both cases (documentation, RTL, test-bench, drivers, other design artifacts • Industry quality
SoC Development Infrastructure	• Focus on standard peripherals	• Focus on High performance accelerators	• Software stack (e.g., OS, libraries, middleware, and applications) • Software development tools (e.g., compilers, linkers, debuggers) • SoC construction tools (e.g., machine-readable IP block descriptions, automated SoC composition and optimization)
Vendor Indepence	• Validate with different colaterals		• Avoid locking of HW-IP and SW-stack/tools to specific vendor

European Commission

KDT JU Key Digital Technologies Joint Undertaking

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TRISTAN and ISOLDE Project

Synergise, Complement and Build a strong European Network

Item	Tristan	Isolde	Comment
Safety/Security		• Especially multi-core • Preparation of certification	• Features enabling Safety and/or Security Certification for high-performance RISC-V Computing
Research		• High Performance Computing research	• ISOLDES‘s focus is high performance compute, TRISTAN‘s focus is SoC building
Open Source (OS)	• Active European OS Hardware Community	• High Quality OS Hardware and Software IP	• Both strive for deliverables given to open source
Demonstration of Building Block Interoperability	• Mainly models and FPGAs • Interoperability between a high number of IPs	• Mainly FPGAs and ASICs • Make OS IPs de factor standard • Focus: Cores and Accelerators	• ASICs and FPGAs are targeted in both projects. Isolde strives for more ASIC demonstrators

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Summary

- TRISTAN & ISOLDE are starting points for creating a **European Eco-System of RISC-V and Open-Source**
- Within 5 years RISC-V CPU's are at no functional disadvantage to establish **competitive & competing architectures**
- TRISTAN & ISOLDE will form the impetus to create low-, mid- and high-end platforms for different **strategic application domains** in Europe...

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Thank you for your attention

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